Power Consumption Simulator for Multi-cores

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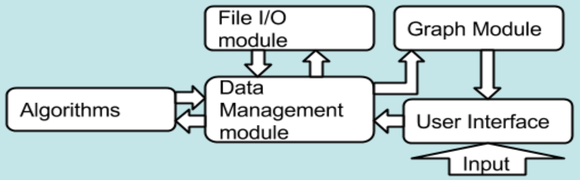
Introduction

❖In order to prove the viability of per core frequency scaling for multicore CPUs, we developed a power simulator that uses real parallel workloads to simulate the power consumption of CPUs with both non-uniform and uniform frequencies.

System Design

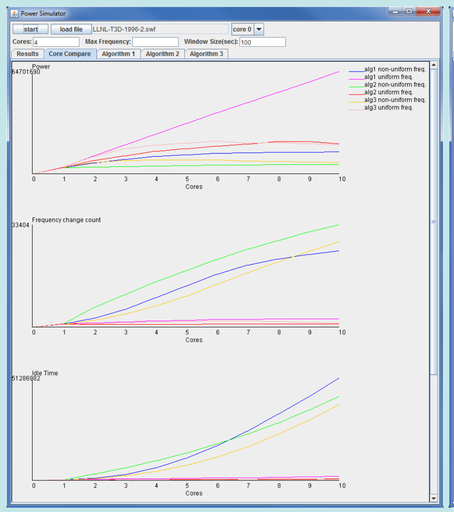
❖System design diagram

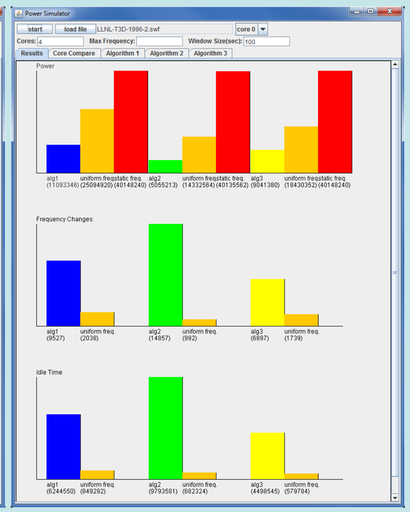


❖Scheduling Algorithms (First Come First Serve)

- Algorithm 1: Finds the first core that can meet the deadline
- Algorithm 2: Finds the core that completes the task at the lowest frequency
- Algorithm 3: Finds the core that completes the task at the lowest frequency. Then finds the best frequency for all tasks in a given window and adjusts them.

❖Power Simulator user interface





Estimated Power

❖"…The power consumed by a core is (typically) proportional to the cube of its frequency" [1] and idle power is roughly 10% [2]

❖Notations

- f: frequency
- F: Task finish time
- M: Number tasks on nth core
- J: Length of uniform frequency schedule
- S: Task start time
- N: Number of cores
- t: run time

❖Simulated non-uniform frequency

- P_1:Estimated power consumed $P_1 = \sum_{n=1}^{N}\sum_{m=1}^{M}(f_{nm}^3 t_{nm})$
- I_1:Idle time $I_1 = \sum_{n=1}^{N}\sum_{m=2}^{M}(F_{n(m-1)} - S_{nm})$
- C_1:Number of frequency changes

❖Simulated uniform frequency

- P_2:Estimated power consumed $P_2 = N\sum_{j=1}^{J}(f_j^3 t_j)$
- I_2:Idle Time $I_2 = N\sum_{j=2}^{J}(F_{j-1} - S_j)$
- C_2:Number of frequency changes

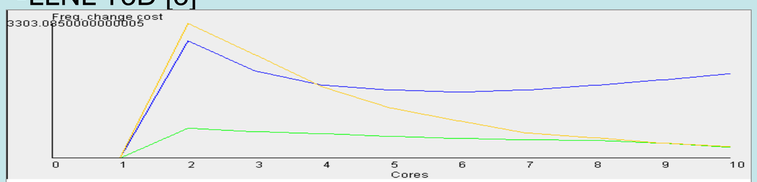
Results

❖Calculated maximum frequency change cost for the viability of CPUs with non-uniform frequencies.

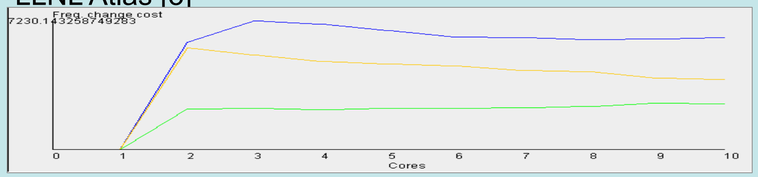
$$x = (P_2 - P_1 + .1(I_2 - I_1)) / (C_1 - C_2)$$

❖Maximum frequency change costs for viable non-uniform frequencies.

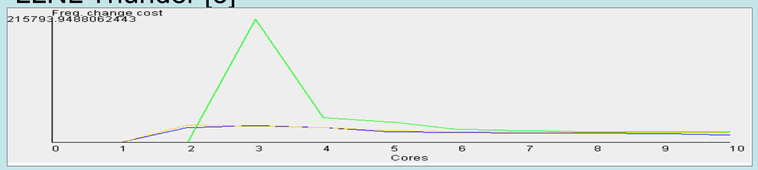
- LLNL T3D [3]



- LLNL Atlas [3]



- LLNL Thunder [3]



Conclusion

❖Power simulation of normalized values shows that non-uniform frequencies may theoretically improve efficiency.

❖Work is going to verify the theoretical results by measuring the real power consumption of multicore processors running a variety of workloads.

Acknowledgment

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References

[1] V. A. Korthikanti, G. Agha, Energy-Bounded Scalability Analysis of Parallel Algorithms. In *Proceedings of the USENIX Workshop on Hot Topics in Parallelism (HotPar)*, 2010.

[2] H. Su, F. Liu, A. Devgan, E. Acar, S. Nassif, Full Chip Leakage Estimation Considering Power Supply and Temperature Variations. In *Proceedings of the International Symposium on Low Power Electronics and Design*, pp 78–83, 2003.

[3] Workload files: LLNL T3D, LLNL Thunder, LLNL Atlas, available at: http://www.cs.huji.ac.il/labs/parallel/workload/logs.html