Electrokinetic flow control in microfluidic chips using a field-effect transistor

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Received 5th January 2006, Accepted 21st April 2006
First published as an Advance Article on the web 11th May 2006
DOI: 10.1039/b600067c

A field-effect transistor is developed to control flow in microfluidic chips by modifying the surface charge condition. In this investigation, zeta potential at a particular location is altered locally by applying a gate voltage, while zeta potential at other locations is maintained at its original value. This non-uniform zeta potential results in a secondary electroosmotic flow in the lateral direction, which is used for flow control in microgeometries. Here, microchannel structures and field-effect transistors are formed on polydimethylsiloxane (PDMS) using soft lithography techniques, and a micro particle image velocimetry technique is used to obtain high resolution velocity distribution in the controlled region. The flow control is observed at relatively low gate voltage (less than 50 V), and this local flow control is primarily due to current leakage through the interface between PDMS and glass layers. A leakage capacitance model is introduced to estimate the modified zeta potential for the straight channel case, and excellent agreement is obtained between the predicted and experimental zeta potential results. This leakage-current based field-effect is then applied to a T-channel junction to control flow in the branch channel. Experiments show that the amount of discharge in the branch channel can be controlled by modulating gate voltage.

Introduction

In the last decade, microfluidic technology experienced exponential growth in bio-analytical areas. This includes DNA sequencing, PCR amplification, protein separation and analysis, immunoassays, cell sorting and manipulation, and in vitro fertilization.[1–3] This development is primarily due to the fact that microfluidic based devices offer rapid separation, automation, minimum sample consumption, and online integration with other unit operations. Generally, complex structured microgeometries such as T-channel, cross-channel, and Y-channel are required to carry out different bio-analytical activities on a single device. Hence a microchannel is preferred over a traditionally-used capillary tube since integrated microfluidic devices can be formed fairly easily using the existing microfabrication techniques.

In microfluidic devices, non-mechanical electroosmotic pumps are most widely used to drive samples because (a) it can be integrated within a single microchip, (b) the flow rate can be controlled very precisely using an externally applied electric field, and (c) it is useful for a wide range of sample conductivity. Electroosmotic flow (EOF) is the bulk motion of ionized liquid with respect to a stationary charged surface under the action of an electrokinetic body force. The magnitude of EOF velocity in a microchannel can be controlled either by changing the external electric field applied along the flow direction or by modifying the electrokinetic potential at the Stern plane (also known as zeta potential, ξ). It is relatively easy to control the flow rate in a microchannel by adjusting the external electric field applied in the flow direction. This kind of control is generally global, and it affects the entire electric field region. However, it cannot be applied to a local area of interest or in complex micro-geometries such as a T-junction or cross-channel junction. On the other hand, selective manipulation of zeta potential has promise to control the flow locally.

The exact manipulation of zeta potential in a microchannel is quite challenging because it depends on solution pH, buffer concentration, and surface charge density. Lee *et al.* first introduced the zeta potential control inside a capillary by applying a gate voltage at the outer surface of the capillary (see ref. 4 and reference therein). They also demonstrated a simple capacitor model to estimate the zeta potential inside the capillary wall. The thickness of the capillary wall in their experiment was 100 μm, so the required gate voltage to obtain a distinct change in zeta potential was on the order of 10^3 V. Control of zeta potential at a relatively low gate voltage can be achieved by either reducing chemical ionization or enhancing the induced charge. Chemical ionization of surface silanol groups can be minimized by using a dilute solution[5] and/or low pH buffer solution.[6] However, the utilization of low pH buffer restricts the applicability of this technique to acidic buffer only. This problem can be overcome to some degree by coating the channel wall. Hayes demonstrated that the coating of capillary walls with large organo silanes gives better control of local zeta potential,[7] and this technique can be used for a wide range of buffer pH. It is important to note however that coating of the channel wall with polymer itself changes zeta potential.[8] Therefore, a careful analysis of zeta potential is necessary when a combination of dynamic coating technique and the gate voltage approach is desired.

To maximize the effects of induced charge *via* externally applied gate voltage, a very thin channel wall (insulator or capacitor) is needed because the wall capacitance is inversely

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proportional to the thickness of the wall (in the case of a rectangular channel). Richard *et al.* fabricated ultra thin silicon nitride layer (390 nm), and exhibited a low gate voltage flow control (on the order of 10 V) in a silicon microchip.[9] They are the first group to report field-effect control using a microchannel rather than capillaries. In their model, three kinds of capacitances (due to channel wall, Stern layer, and diffuse layer) were considered, and they pointed out that saturation occurs at high gate voltage due to the fact that the capacitance of electric double layer (EDL) also increases with the applied secondary (perpendicular) electric field. Later Buch *et al.* demonstrated field-effect flow control in a PDMS microchannel with a 2 μm thick silicon dioxide capacitor.[10] Karnik *et al.* examined the effects of perpendicular electric field originated from gate voltage in a nanofluidic channel. They found that both zeta potential and ionic concentration are influenced when the channel size is comparable to or smaller than the Debye length.[11] Lately, field effects were utilized in silicon microchips to obtain non-uniform zeta potential for micromixing[12] and localized dispersion control.[13]

So far field-effect transistors or capacitors are formed either on glass or silicon wafer to control the flow in microchannels or capillaries. However, it has not been attempted on polymeric materials, although polymeric materials are extremely popular in "lab-on-a-chip" devices. Moreover, none of the above-mentioned articles discussed current leakage of the capacitor assuming a perfect insulating channel wall. In practice, most dielectric materials used in electrokinetic based microfluidic applications allow current leakage, especially at high electric field. Therefore, the main objective of this study is to demonstrate localized flow control in micro-geometries using a leakage-current based field-effect transistor formed on PDMS. We also present a detailed theoretical model for leakage-current to estimate the zeta potential in the controlled region. In this study, a high resolution micro particle image velocimetry (μPIV) technique is utilized to obtain detailed velocity distribution in the controlled region. The resultant velocity distributions tell us the potential applicability of our proposed field-effect control mechanism in a hybrid PDMS–glass microchannel.

Theory

Field-effect transistor design and leakage capacitance model

The field-effect controlled microchip, shown in Fig. 1, consists of two perpendicular channels with a micron-sized separation between them. The main (horizontal) channel between drain and source reservoirs is filled with a target liquid or sample. A net flow of sample can be achieved by applying an electric field along the direction of source to drain reservoir. The sub-channel is formed to apply a perpendicular electric field for field-effect flow control, and this channel is filled with a stationary conductive liquid. The voltages at the drain and gate reservoirs are set as V_d and V_g, respectively, while the source reservoir is connected to a common ground. In this investigation, both main and sub-channels are filled with 100 mM borate buffer, though it is possible to fill these channels with any ionized liquid.

When borate buffer comes into contact with the channel (PDMS) wall, the channel surface becomes negatively charged due to the ionization, ion absorption, or ion adsorption. To maintain electroneutrality in the system, counter ions from the liquid are attracted to the wall forming an immobilized Stern layer (see inset in Fig. 1). The next layer is known as the diffuse layer where ions are subjected to both electrostatic potential energy and thermal kinetic energy. The thickness of this diffuse layer is generally quantified by a characteristic

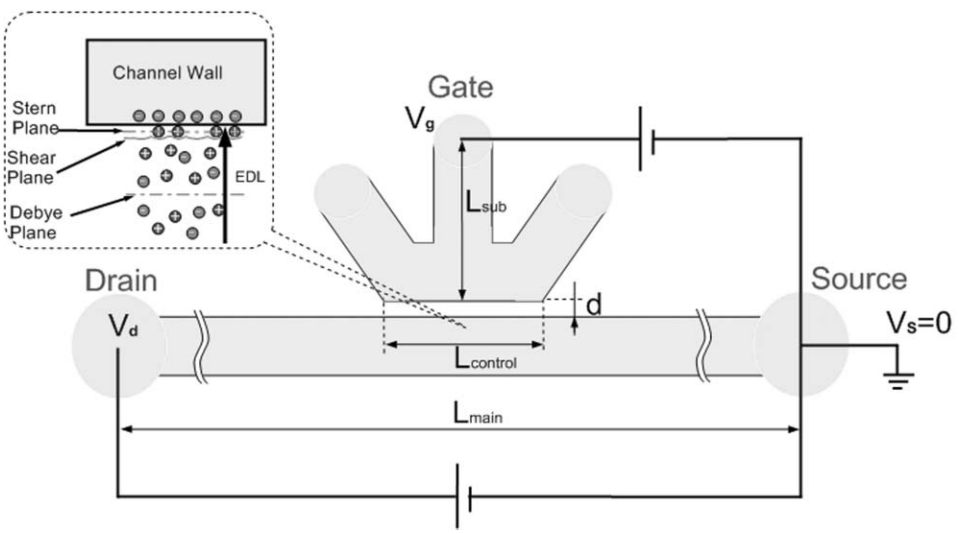

Fig. 1 Schematic view of a field-effect controlled microfluidic device for straight channel application. The main (horizontal) channel is separated from the sub- (vertical) channel by a micron sized distance (d). The potentials at drain and gate reservoirs are V_d and V_g, respectively, while the source reservoir is connected to a common ground ($V_s = 0$). The length of main channel (L_{main}), sub-channel (L_{sub}), and control region ($L_{control}$) is 2 cm, 2.5 mm, and 1 mm, respectively. In this study, drain voltage is fixed at 50 V, while the gate voltage is modulated between 5 V and 45 V. The inset shows the formation of the EDL next to the channel surface.

dimension called Debye length (λ). For symmetric ionic valences ($z_+ = -z_- = z$), Debye length is given by[14]

$$\lambda = \sqrt{\frac{\varepsilon_b \varepsilon_0 RT}{2z^2F^2c_\infty}} \quad (1)$$

where ε_b is the relative permittivity of the buffer solution, ε_0 is the permittivity of free space, R is the universal gas constant, T is the absolute temperature, F is the Faraday constant, and c_∞ is the ionic concentration in the bulk region. Stern and diffuse layers together form the EDL. The thickness of the Stern layer is generally much smaller than the diffuse layer. Hence, in this study, the effects of Stern layer are neglected in the EDL phenomena and capacitance estimation; the capacitance of the diffuse layer is referred to as EDL capacitance hereafter.

Fig. 2(a) illustrates the equivalent electric circuit of our field-effect flow controller. Due to the presence of two fluidic channels, there are three different capacitors in this system: EDL capacitor of the sub-channel (C_{EDL1}), wall capacitor (C_{wall}), and EDL capacitor of the main channel (C_{EDL2}). The capacitance of an EDL can be expressed as[14]

$$C_{EDL} = \frac{\varepsilon_b \varepsilon_0 A}{\lambda} \cosh\left(\frac{zF\zeta}{2RT}\right) \quad (2)$$

where A is the charged area. In a straight microchannel, one can determine the value of ξ by measuring the EOF velocity (u_{eo}) using

$$\zeta = -\frac{u_{eo}\mu}{E\varepsilon_b\varepsilon_0} \quad (3)$$

where E is the electric field and μ is the viscosity of the fluid. The capacitance of the separation wall is given by

$$C_{wall} = \frac{A\varepsilon_w\varepsilon_0}{d} \quad (4)$$

where ε_w is the relative permittivity of the wall material and d is the separation distance between the main and sub-channels. Since all three capacitors are in series, the total capacitance can be calculated as

$$C_{total} = [C_{wall}{}^{-1} + C_{EDL1}{}^{-1} + C_{EDL2}{}^{-1}]^{-1} \quad (5)$$

In a particular microfluidic system, if the thickness of the wall is much larger than the Debye length, the order of magnitude of the C_{wall} is smaller than C_{EDL}. This implies that C_{wall} is the dominating term in C_{total}.

Due to the presence of gate voltage (V_g), the zeta potential at the controlled region will change from its original (reference) value. The change in zeta potential at the controlled wall can be expressed as[4]

$$\Delta\zeta = \zeta - \zeta_0 = -\frac{C_{total}}{C_{EDL2}}\Delta V_C = -\frac{C_{total}}{C_{EDL2}}(V_C - V_{C0}) \quad (6)$$

where V_C is the voltage across the total capacitor. The subscript "0" stands for the reference state for which there is no control of zeta potential. Eqn (6) indicates that the use of diluted solution and/or ultra thin wall thickness (d) enhances the influence of ΔV_C on $\Delta\xi$. For the no-leakage capacitance model, used in earlier studies,[4,12,13] the applied voltage across the total capacitor can be estimated from the difference in the gate voltage and the local fluid voltage. However, in this study we observed current leakage from the sub-channel to the main channel due to improper bonding and/or finite surface roughness ($\sim$150 nm) of channel materials. This is consistent with the observation of Hayes *et al.*[6] Therefore, the estimation of applied voltage across the total capacitance requires consideration of leakage-current.

To fully understand the effects of leakage-current in the zeta potential modification, we introduced a leakage capacitance model considering an effective resistance parallel to the capacitors as shown in Fig. 2(a). Note that if there were no current leakage (so-called perfect capacitor), the leakage resistance would be infinite ($R_{leak} \to \infty$). For simplicity the

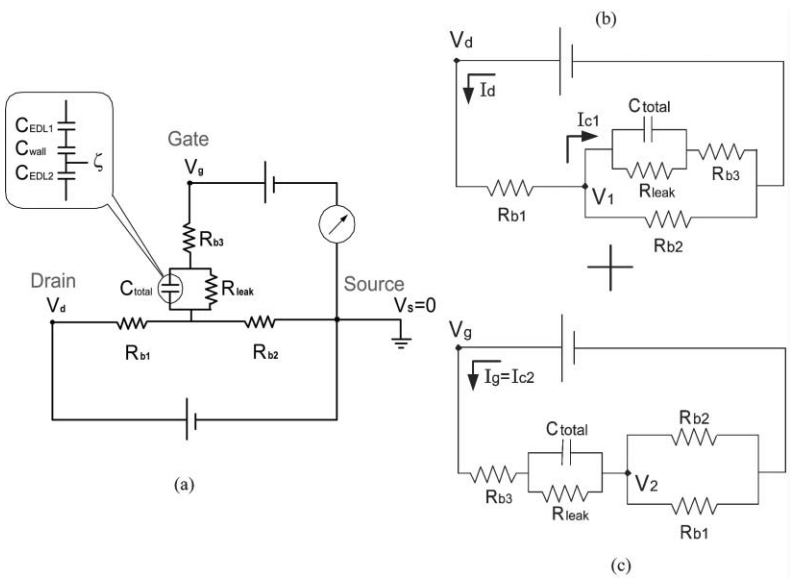

Fig. 2 (a) Equivalent electric circuit of field-effect controlled microfluidic device shown in Fig. 1. A leakage capacitance model is considered due to the presence of leakage current through the capacitor. The capacitance of the Stern layer is neglected in the present study because the diffuse layer dominates the EDL capacitance. (b) and (c): Linear decomposition of (a) for drain voltage and gate voltage, respectively.

electrical circuit presented in Fig. 2(a) is decomposed into two separate circuits as shown in Fig. 2(b) and (c). Now we analyze the two separate circuits in order to determine applied voltage across the total capacitor. In Fig. 2(b), the current through resistance R_{b1} can be calculated as

$$I_d = \frac{V_d}{R_{b1} + (R_{b3} + R_{leak})||R_{b2}} \quad (7)$$

where the notation, ||, is employed to simplify the equivalent resistance in parallel (*i.e.* $R_A||R_B \equiv R_A R_B/(R_A + R_B)$). Also from Fig. 2(b), the current passing through the sub-channel resistance (R_{b3}) is

$$I_{c1} = \frac{R_{b2}}{R_{b2} + (R_{b3} + R_{leak})} I_d \quad (8)$$

Therefore, the voltage at the center of the channel (V_1) can be analytically solved as

$$V_1 = \frac{(R_{b3} + R_{leak})||R_{b2}}{R_{b1} + (R_{b3} + R_{leak})||R_{b2}} V_d \quad (9)$$

Similarly, in Fig. 2(c), the current through the sub-channel can be found as

$$I_{c2} = I_g = \frac{V_g}{(R_{b3} + R_{leak}) + R_{b1}||R_{b2}} \quad (10)$$

and the potential at the controlled region (V_2) can be calculated as

$$V_2 = \frac{R_{b1}||R_{b2}}{(R_{b3} + R_{leak}) + R_{b1}||R_{b2}} V_g \quad (11)$$

Note that the current direction I_{c1} is opposite of I_{c2}. In the no-control case, there is no net current through the leakage resistance ($I_{c1} = I_{c2}$), and the corresponding gate voltage (reference gate voltage) can be found as

$$\begin{aligned} V_{g0} &= V_g\big|_{I_{c1} = I_{c2}} \\ &= \frac{R_{b2}}{R_{b2} + (R_{b3} + R_{leak})} \frac{(R_{b3} + R_{leak}) + R_{b1}||R_{b2}}{R_{b1} + (R_{b3} + R_{leak})||R_{b2}} V_d \end{aligned} \quad (12)$$

Thus the voltage change across the capacitance for any modulation of gate voltage is given by

$$\begin{aligned} \Delta V_C &= R_{leak}(I_{C2} - I_{C1}) = \frac{R_{leak}(V_g - V_{g0})}{(R_{b3} + R_{leak}) + R_{b1}||R_{b2}} \\ &= \frac{R_{leak}}{(R_{b3} + R_{leak}) + R_{b1}||R_{b2}} \Delta V_g \\ &= R_{leak}\left[\frac{V_g}{(R_{b3} + R_{leak}) + R_{b1}||R_{b2}} - \right. \\ &\left. \frac{R_{b2}}{R_{b2} + (R_{b3} + R_{leak})} \frac{V_d}{R_{b1} + (R_{b3} + R_{leak})||R_{b2}}\right] \end{aligned} \quad (13)$$

where $\Delta V_g = V_g - V_{g0}$. The above relation implies that the voltage change across the capacitor (ΔV_C) increases as ΔV_g increases. Hence, in our leakage capacitance model, the zeta potential change can be estimated as

$$\Delta\zeta = -\left(\frac{C_{total}}{C_{EDL2}}\right)\left(\frac{R_{leak}}{(R_{b3} + R_{leak}) + R_{b1}||R_{b2}}\right)\Delta V_g \quad (14)$$

Therefore, in order to obtain flow control in a straight microchannel ΔV_g must be non-zero.

Experimental

Fabrication of field-effect controlled microfluidic device

In this study, reservoirs and open microchannel structures are formed on PDMS using standard soft lithography techniques,[15] and a thin cover glass slide is used to close the channel from the bottom. Alternatively, another PDMS layer could have been fabricated as the bottom layer for this device. Even though both glass and PDMS are suitable materials for electrokinetic flow, the glass slide is chosen over PDMS to obtain high resolution velocity distribution in the microchannel using μPIV technique.

The microfabrication sequence consists of photolithography and replica molding. In the photolithography step, positive photoresist (AZP4620, AZ Electronic Materials, NJ USA) is first spin-coated on a silicon wafer at 2000 rpm for 19 s, which results in a 10 μm thick layer. Next, a patterned positive relief is prepared by exposing the desired part of the photoresist (using a mask) to near ultraviolet light for 60 s and then dissolving the exposed regions with the appropriate developer (AZ400, AZ Electronic Materials, NJ USA). Meanwhile, the PDMS prepolymer and the curing agent (Sylgard 184, Dow Corning Inc., MI USA) are mixed at a ratio of 10:1. The mixed liquid elastomer is then degassed for 2 h at 0.001 Torr and cast onto the prepared substrate after placing capillaries at the drain, source, and gate reservoir positions. The PDMS is then cured by an organometallic crosslinking reaction for 6 h at 80 °C in a hot oven. The solidified PDMS is peeled off and capillaries are taken out to have reservoirs in the PDMS. The resultant slab is the top layer of the microchannel. As mentioned earlier, a cover glass is used as the bottom layer in this study. For permanent bonding of top and bottom layers, both PDMS and glass layers are illuminated by oxygen RF plasma (PDC-32G, Harrick Scientific Co., NY USA) for 20 s prior to the bonding. Oxygen plasma treatment renders the PDMS surface hydrophilic. This facilitates easy loading of sample due to the replacement of CH_3-groups with OH-groups.

Optical detection system

The localized flow control phenomena are monitored and quantified using fluorescent based micro particle image velocimetry (μPIV) technique. This is one of the most powerful methods to obtain both qualitative and quantitative velocity distributions in a microchannel with high resolution. The μPIV detection system used in this study, as shown in Fig. 3, has a spatial resolution of 5.36 μm.[16] It consists of Nd:YAG laser, CCD camera, optical components (neutral density filter, beam expander, dichroic mirror, color filters, and 20× objective lens), synchronizer, and data acquisition system. The intensity of the laser (Nd:YAG Powerlite, Continuum, CA USA) is reduced to 10 mJ by using neutral density filter (FSR-OD80, CA USA). A Galilean type beam expander, composed of two lenses (01LPK007/078 and 01LAO256/078, Melles Griot, CA USA), is placed to guide the light into an inverted fluorescent

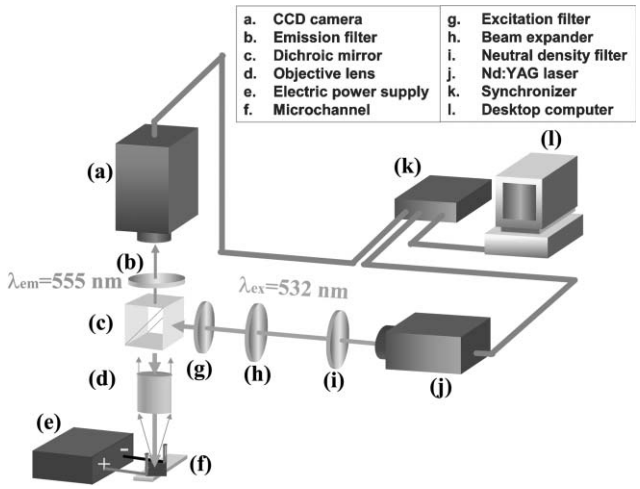

Fig. 3 Experimental setup for μPIV technique. The modified carboxyl seeding tracers are excited at 540 nm and emit light at 560 nm of wavelength. The cooled CCD camera with 1280 × 1024 pixels provides 1280 instantaneous vectors. For a 20× magnification objective lens, the spatial resolution of our PIV system is 5.36 μm × 5.36 μm with a depth of field δz = 13.18 μm.

microscope (CKX41, Olympus Co., Tokyo Japan), which is equipped with the cooled CCD camera (PIVCAM13-8, TSI Inc., MN USA). In this study, 500 nm orange fluorescent (540 nm excitation and 560 nm emission) polystyrene microspheres (Molecular Probes, OR USA) are used as seeding particles. Since the orange fluorescent seeding particles have a very narrow wavelength difference between excitation and emission, a special dichroic cube (Z532/10, 532RDC, HQ575/50) is installed in the optical path. The concentration of the tracer particles is adjusted to have 10 particles per interrogation area (10.72 μm × 10.72 μm). In our experimental setup, the depth of field (δz = 13.18 μm) is higher than the microchannel height. Hence, the velocity distributions presented in this study are depth wise average values.

Results and discussion

Reasons for using low gate voltage

Since EOF velocity is directly related to the zeta potential (ξ), the maximum flow control can be achieved by increasing $\Delta\xi$. However, eqn (14) indicates that the effect of gate voltage on the zeta potential change is not straightforward. As the gate voltage increases, the capacitance of EDL2 (EDL at the controlled region in the main channel) also increases and saturation occurs at high gate voltage.[9] Moreover, at very high gate voltage (on the order of 10^3 V) an enormous amount of current passes through the 50 μm thick PDMS wall because the breakdown voltage of PDMS is relatively low. Our experiments indicated that the dielectric strength of the PDMS is 21.18 V μm^{-1} (7.2 kV for 340 μm), which agrees with the specification of Sylgard 184 provided by the Dow Corning Corporation.[17] The large current of high electric field can easily open the disconnected region (capacitors in our model), and the fluid eventually leaks into the pathway. Application of this single-use-valve has been introduced by McDonald *et al.*[18] However, at low electric field strength there is no fluid leakage, so our model is useful when the gate voltage difference (ΔV_g) is less than 100 V.

Origin of current leakage at low gate voltage

Two separate experiments have been performed to identify leakage sources in our microfluidic chip. The overall setting of these experiments is identical to the one shown in Fig. 1, where positive voltages are applied in gate and drain reservoirs, and the source reservoir is connected to a common ground. The first experiment is designed to make sure that there is no fluid leakage from the sub-channel to the main channel. In this experiment, dye (Rodamine) is mixed with 100 mM borate buffer solution in the sub-channel, whereas the main channel is filled with 100 mM borate buffer only. For an applied gate voltage of 100 V (corresponding electric field, 80 V cm^{-1}) and zero drain voltage for 5 h, no fluid leakage was observed in the main channel, though a measurable current of 20 nA was leaking from the sub-channel to the main channel. The current leakage is monitored using a precise current meter (Keithley Instruments, Inc., Model 6487) placed between gate-source electric circuit as shown in Fig. 2(a). These experiments were repeated for higher gate voltages up to 300 V, and no penetration of dyes to the main channel was observed.

The purpose of the second experiment is to confirm whether the current leakage behavior is universal in our microfluidic system or if it is only due to the presence of conductive liquid in the sub-channel. In order to verify this, the sub-channel is filled with a 2.5% w/w agarose gel instead of borate buffer. Note that the gel is preheated at 80 °C in water before loading, and then the entire chip is cooled to 2 °C for 3 min to solidify the gel. We observed the current leakage phenomena in this experiment too, although the agarose gel required a slightly higher gate voltage (approximately 20 V higher) compared to the borate buffer because of its higher resistance. The results of these two experiments conclude that current passing takes place regardless of choice of materials (borate buffer or agarose gel) used in the sub-channel, and there is no fluid leakage through the 50 μm PDMS wall.

Next, we study the effects of gate voltage (V_g) on the leakage-current behavior. A separate experiment is conducted to determine the resistance of the leakage region by applying only control voltage (V_g) at the gate reservoir. In this experiment, both the primary and sub-channels are filled with 100 mM borate buffer, the source reservoir is connected to ground, and the electrode at drain reservoir is kept electrically floating (V_d = 0). In this configuration, there is no current through the resistance at the left-half of the main channel ($R_{b1} \rightarrow \infty$ and I_d = 0), and the current at the leakage resistance is recorded with a precision current meter. Experimental results show a linear relationship as

$$I_g = 0.2079 V_g - 1.0946 \quad (15)$$

where I_g is the measured current in nanoamperes (nA) and V_g is the gate potential in volts (V). The intercept in eqn (15) is not zero because PDMS behaves like perfect capacitor at low voltage. Note that the inverse of slope in eqn (15) represents

the total resistance (R_{total} = 1/0.2079 GΩ). Therefore, the resistance of leakage region (R_{leak}) can be estimated as

$$R_{leak} = R_{total} - (R_{b2} + R_{b3}) \quad (16)$$

where R_{b2} and R_{b3} are the resistances of the borate buffer in the right-half of the main channel and sub-channel, respectively. The value of the R_{b2} and R_{b3} are calculated from the specific resistivity of borate buffer (ρ_{borate} = 1.83 Ω m) and channel geometries (see Fig. 1) as 12.2 MΩ and 2.94 MΩ, respectively. Therefore, the resulting leakage resistance becomes 4.795 GΩ. Now, if we assume that the 50 μm thick PDMS wall allows current leakage, the resistivity of the wall material for this experiment becomes 0.96 × 10^6 Ω m. This value is significantly small compared to the resistivity of bulk PDMS (1.2 × 10^{12} Ω m[17]). It may be due to the existence of nano-pores at the interface between PDMS and glass. In this experiment, the roughness of the plasma-treated PDMS and the cover slip are calculated as 150 nm and 30 nm, respectively. The oxidized PDMS surface has a relatively large roughness, so even after bonding with the other layer tiny gaps still exist which traps some portion of liquid when the buffer solution is loaded. This hypothesis explains why the single-use-valve of McDonald *et al.*[18] opens from the interface between two layers. In other words, the interface has the weakest resistance against the flow of electrons. Each nano-pore seems to have approximately 30 nm width. Since the smallest thickness dominates the total value of the wall capacitance, we regard the minimum size of these nano-pores as the effective thickness of the capacitor.

Time dependence consideration

In this section we analyze the time scale for the control voltage (V_C) to achieve steady state. A finite amount of time will be required to establish the steady voltage across the capacitors since a leakage capacitance model is used in this study. To analyze the transient time scale, an equivalent electrical circuit corresponding to gate voltage circuit (in Fig. 2(c)) is presented in Fig. 4. Using Thevenin's theorem, one can simply convert any linear circuit to an equivalent circuit of one voltage source, one series resistance, and a load component.[19] In our case, we first regard the capacitor as the load and remove it temporarily from the circuit to find Thevenin voltage. The voltage across the load terminal (Thevenin voltage) is V_{thev} = 0.998 V_g. Now the Thevenin resistance is the effective resistance as seen from the load terminals without having all power sources in the original circuit. Therefore, the Thevenin resistance of this circuit is determined as

$$R_{thev} = (R_{b1} \parallel R_{b2} + R_{b3}) \parallel R_{leak} \quad (17)$$

In the above analysis, the contribution of drain loop (Fig. 2(b)) is not considered because the same drain voltage is maintained in order to determine the effects of the gate voltage only. In Fig. 4, the voltage that appears across the capacitor after the power supply is turned on is given by[19]

$$V_C = V_{thev}(1 - e^{-t/(R_{thev}C_{total})}) \quad (18)$$

Therefore, at time $t = 4.8R_{thev}C_{total} \approx 10.4$ μs, the voltage across the capacitor became 99.0% of the original voltage (V_g) where $C_{total} \approx 0.24$ pF. With time, the voltage across the capacitor reaches 99.8% of V_g. Because all the velocity data are acquired after 30 s from the initiation of the gate voltage, we neglect the time dependency of our experimental data.

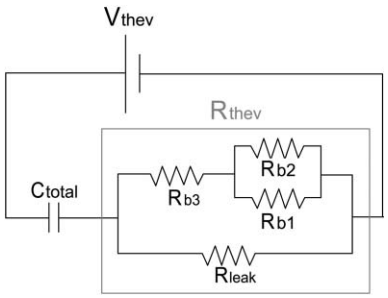

Fig. 4 Equivalent circuit of Fig. 2(c) based on Thevenin's theorem. The total capacitor is treated as the reactive component. Here the Thevenin voltage is $R_{leak}/\{R_{b3} + R_{leak}) + R_{b1} \parallel R_{b2}\}\Delta V_g$, and the Thevenin resistance is $(R_{b1} \parallel R_{b2} + R_{b3}) \parallel R_{leak}$.

Flow control in a straight channel

The experimental setup for flow control in a straight channel is shown in Fig. 1. Here the length of main and sub-channels is 2 cm and 2.5 mm, respectively, and both main and sub-channels are 150 μm wide and 10 μm deep. To our knowledge, we are the first group to investigate the point-wise velocity distribution inside a field-effect-controlled microchannel using micro particle image velocimetry (μPIV) technique. In the μPIV technique, sub-micron sized fluorescent particles are seeded with buffer solution to track microflow. These seeding particles are generally negatively charged due to the presence of a carboxyl group (–COOH) at their surfaces. Hence, electrophoretic mobility of seeding particles is measured prior to the flow control experiment.

The electrophoretic velocity of seeding particles under an applied electric field can be estimated as[14]

$$\vec{u}_{PH} = -\frac{ze}{3\pi d_P \mu}\nabla\phi = -M_{PH}\nabla\phi \quad (19)$$

where d_p is the particle diameter, $\nabla\phi$ is the electric field acting on the particle, and M_{PH} is the electrophoretic mobility. In order to estimate the electrophoretic velocity in our microfluidic system, the wall surface is coated with methylcellulose (1.1% w/w MC) before loading the buffer solution and tracer particles into the channel. In this experiment, the mean electrophoretic mobility of the seeding particles is determined as $M_{EP} = -1.3965 \times 10^{-4}$ cm^2 V^{-1} s^{-1}.

Next, the electroosmotic mobility of 100 mM borate buffer is obtained in a glass–PDMS straight channel by subtracting the measured electrophoretic velocity from the observed flow field. The resultant electroosmotic mobility is 2.3890 × 10^{-4} cm^2 V^{-1} s^{-1}. Therefore, the Debye length and the zeta potential under no-control conditions are calculated as $\lambda \approx 0.962$ nm and $\xi \approx -35.4$ mV, respectively using the following flow properties (ε_0 = 8.8541878176 × 10^{-12} F m^{-1}, $\varepsilon_b \approx \varepsilon_{water}$ = 78.5, z = 1, R = 8.3144 J mol^{-1} K^{-1},

T = 25 °C = 298.15 K, F = 96485.3415 C mol^{-1}, c_∞ = 100 mM, μ = 1.025 × 10^{-3} Pa s).

For the field-effect control experiment, both main and sub-channels are filled with 100 mM borate buffer, and potentials are applied in the drain and the gate reservoirs using platinum electrodes. The length of the control region is 1 mm (shown partially at the top in Fig. 5(b)), and it is located between x = −350 μm and x = 650 μm. In this study the gate voltage is modulated between 0 V to 45 V by keeping the drain voltage at a fixed value. There are two reasons for not applying higher gate voltages in this study. First, the EDL capacitance (C_{EDL2}) changes with the zeta potential, hence, saturation is expected to be seen at higher gate voltages. Second, seeding particles, used to track the flow, get attracted to the control wall at higher gate voltages. This creates a nonuniform particle distribution that can cause inaccurate PIV vector calculations. Hence, we present the flow control at low gate voltage ($|V_g| < 45$ V), and no reverse flow is observed due to the fact that the zeta potential never reaches positive value.

Figs. 5(a) and (b) demonstrate the field-effect EOF results inside a straight microchannel for the no-control (ΔV_g = 0 V) and control (ΔV_g = 20 V) cases, respectively. As mentioned earlier, in all flow results, the electrophoretic velocity

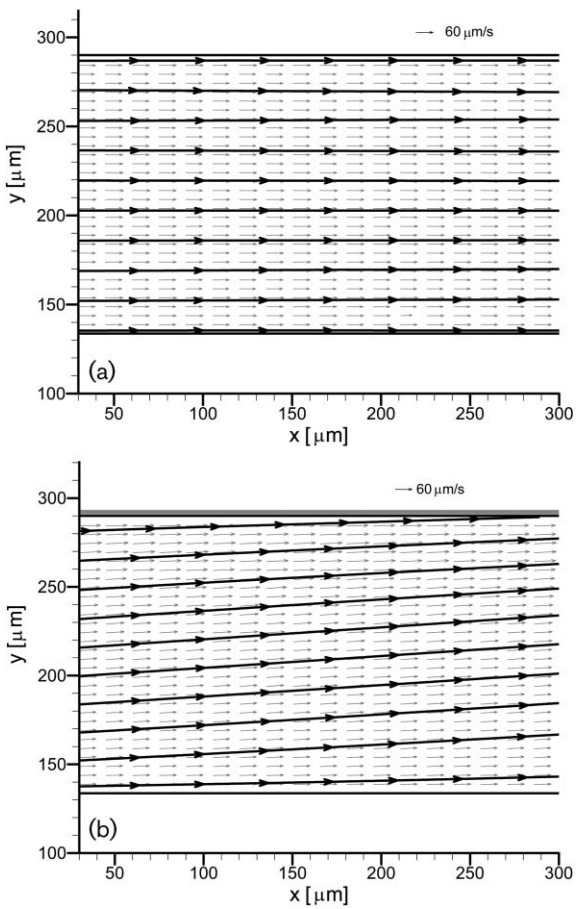

Fig. 5 The velocity distribution inside a straight channel for (a) no-control (ΔV_g = 0 V) and (b) control (ΔV_g = 20 *V*) cases. The control wall is located at y = 290 μm. Here, the drain voltage (V_d) is 50 V, and the gate voltage (V_g) is adjusted at 25 V and 45 V for no-control and control cases, respectively.

contribution is subtracted from the observed flow velocity obtained from μPIV technique. In these experiments we were not able to capture the flow vector in the EDL regions because the spatial resolution of our μPIV system is 5.36 μm for a 20× objective lens. Therefore, the experimental results show velocity close to the wall, but not at the wall. Here the drain and source voltages are kept constant at 50 V and 0 V. Eqn (14) indicates that no change in zeta potential ($\Delta\xi$ = 0) will occur if there is zero current through the leakage resistance. For the above mentioned experimental setup, this can be achieved for a gate voltage of ∼25 V. Hence, the gate voltage for the control case, presented in Fig. 5(b), becomes 45 V and the corresponding zeta potential at the controlled wall is −45.4 mV. Here we expect that potential at the other side of the wall is not significantly affected by the gate voltage due to thermal diffusion layer in EDL, and the zeta potential at uncontrolled wall is assumed to be −35.4 mV. This zeta potential difference across the main channel contributes to lateral velocity in the microchannel toward the controlled region (as seen in Fig. 5(b)). On the other hand, no such lateral velocity is observed in Fig. 5(a) due to the same zeta potential at both sides of the walls. It is noteworthy to mention that the field-effect transistor formed on PDMS is able to alter the zeta potential effectively at very low gate voltage even for a relatively thicker (50 μm) channel wall. This low gate voltage flow control was possible due to the current leakage through the interface between PDMS and glass layers.

Fig. 6(a) shows the stream-wise velocity profile across the main channel for different values of ΔV_g. Experimental evidence indicates that the EOF velocity in the control case is significantly different from that of no-control case (ΔV_g = 0). We also compared our experimental results with the leakage model prediction (in Table 1); excellent agreement is obtained between experimental values and theoretical predictions. As expected, for ΔV_g = 0, the stream-wise velocity is almost uniform throughout the channel. In this case the electro-osmotic mobility (M_{EOF} = 2.3890 × 10^{-4} cm^2 V^{-1} s^{-1}) is identical to that of a pure EOF in a PDMS-glass micro-channel.[16] For the no-control case, the deviation from the uniform profile can be explained from the following facts. In the flow velocity estimation the mean electrophoretic velocity is subtracted from the observed velocity under the assumption that the seeding particles are distributed uniformly, and they have identical charges and sizes. In practice, each particle experiences slightly different electrophoretic migration.

The cross-stream velocity distribution across the channel for different values of ΔV_g is depicted in Fig. 6(b). For the planar channel considered in this study, the value of cross-stream velocity is almost uniform (except at the wall region) for a particular ΔV_g. In the vicinity of the wall, the velocity approaches zero due to no penetration at the side walls. The deviation from the exact uniform profile might be related to the procedure used in eliminating electrophoretic contributions. For positive values of ΔV_g, the cross-stream velocity is positive because the electrokinetic force acts toward the controlled wall, and *vice versa* for negative values of ΔV_g. It is also clear that the magnitude of cross-stream velocity is proportional to the lateral electric field generated due to the change in zeta potential at the side walls. These findings are

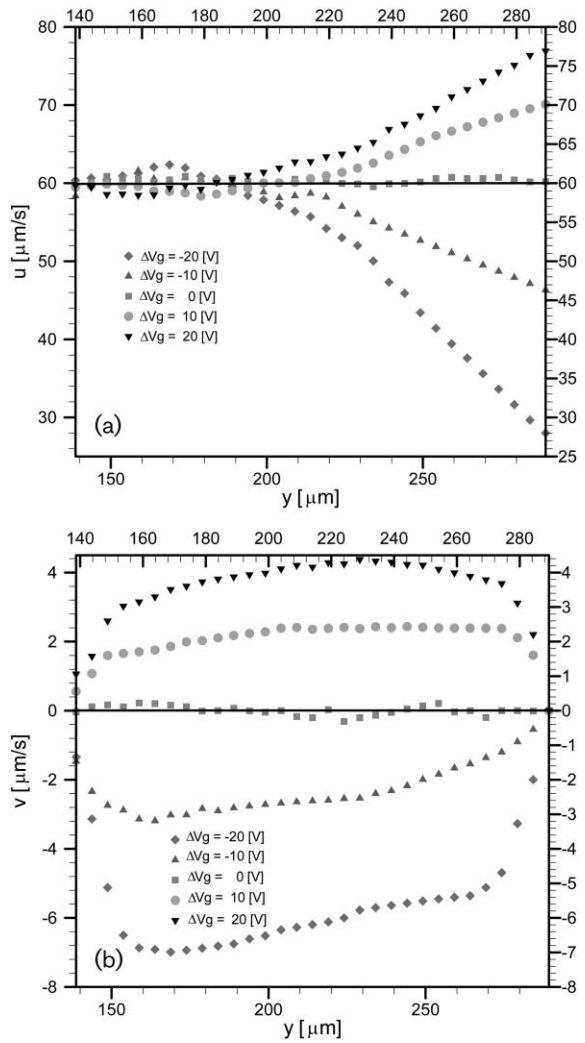

Fig. 6 (a) Stream wise (u) and (b) cross-stream (v) velocity distribution across the straight (main) channel for different values of gate voltage at $x = 175$ μm. Here the reference gate voltage (V_{g0}) is $\sim$25 V.

consistent with the existing electrokinetic theory where EOF velocity is linearly proportional to the applied electric field.

Flow control at a T-junction

T-junctions are widely used in microfluidic based "lab-on-a-chip" devices for sample extraction or loading. Although a T-junction is an essential component of a microfluidic chip for automated sample handling, it is one of the major sources of dispersion in microfluidic devices. The primary reason for band dispersion at a T-junction is the deformation (bending) of electric field lines as current passes by the branch channel.[20] This phenomenon is also evident in a cross-channel junction.[21] Lately Lin *et al.* presented on-chip microelectrode arrays to reshape the electric field lines in a cross-channel junction.[22] In this study a field-effect transistor is used to keep the electric field lines straight in a T-channel junction. The schematic for the T-junction experiments is presented in Fig. 7(a). The drain and gate reservoirs are connected to positive voltages, the source reservoir is connected to a common ground, and the branch channel reservoir is electrically floating. Initially the pressure head at each reservoir is maintained at the same value so that there is no movement of the fluid before applying an external electric field.

Fig. 7(b) shows the fluid flow behavior for the no-control scenario. In this case, the drain voltage is set to 48 V and the gate voltage is fixed at 25 V. This gate voltage corresponds to an equilibrium state in which the leakage-current between the gate and source/drain is zero; we call this the reference gate voltage, V_{g0}. The streamlines (black solid lines), presented in Fig. 7(b), show the direction of the flow in both the main and branch channels for above-mentioned electrical condition. This implies that pressure is induced along the main channel due to electroosmotic pumping action, and the balance of the pressure among the three reservoirs was broken.

Now to control the flow, we intentionally create a leakage current by changing the value of the gate voltage from its equilibrium state. Like the aforementioned straight channel experiment, this leakage-current modifies the zeta potential in the controlled region. The change in the zeta potential on one side of the channel wall will result in a transverse electric field, which will create a cross-stream velocity component. Fig. 7(c) shows velocity vector distribution in a control case for which the gate voltage is 18 V ($\Delta V_g = -7$ V). For this case, almost no sample leakage to the branch channel is evident, and this specific scenario is particularly useful if one desires to transport the sample plug through a T-junction with minimum band distortion. Here the field-effect flow at the T-junction acts like an electro-switching valve using the benefit of this cross-stream velocity component. Thus, the ability to control the cross-stream velocity component at a particular surface plays an important role in obtaining the desired flow pattern.

It is worthwhile to mention that by changing the value of ΔV_g one can also precisely control the amount of the fluid entering into the branch channel. For example, any increase in gate voltage from its reference value ($\Delta V_g > 0$) will result in

Table 1 Comparison of theoretical and experimental zeta potentials at the controlled surface in straight channel application. $V_{control}$ is the velocity in the vicinity of the controlled region

					Zeta potential at the controlled wall (ξ)/mV	
Gate voltage/V	ΔV_g/V	(C_{EDL2}/A (theory)) /F m^{-2}	(C_{Total}/A (theory)) /F m^{-2}	$V_{control}$/μm s^{-1}	Experiment	Theory
5	−20	8.770×10^{-1}	8.101×10^{-4}	28.00	−16.5	−17.2
15	−10	1.186	8.105×10^{-4}	47.00	−27.7	−28.8
25	0	1.524	8.108×10^{-4}	60.00	−35.4	−35.4
35	10	1.875	8.109×10^{-4}	70.00	−41.3	−39.9
45	20	2.178	8.110×10^{-4}	77.00	−45.4	−43.4

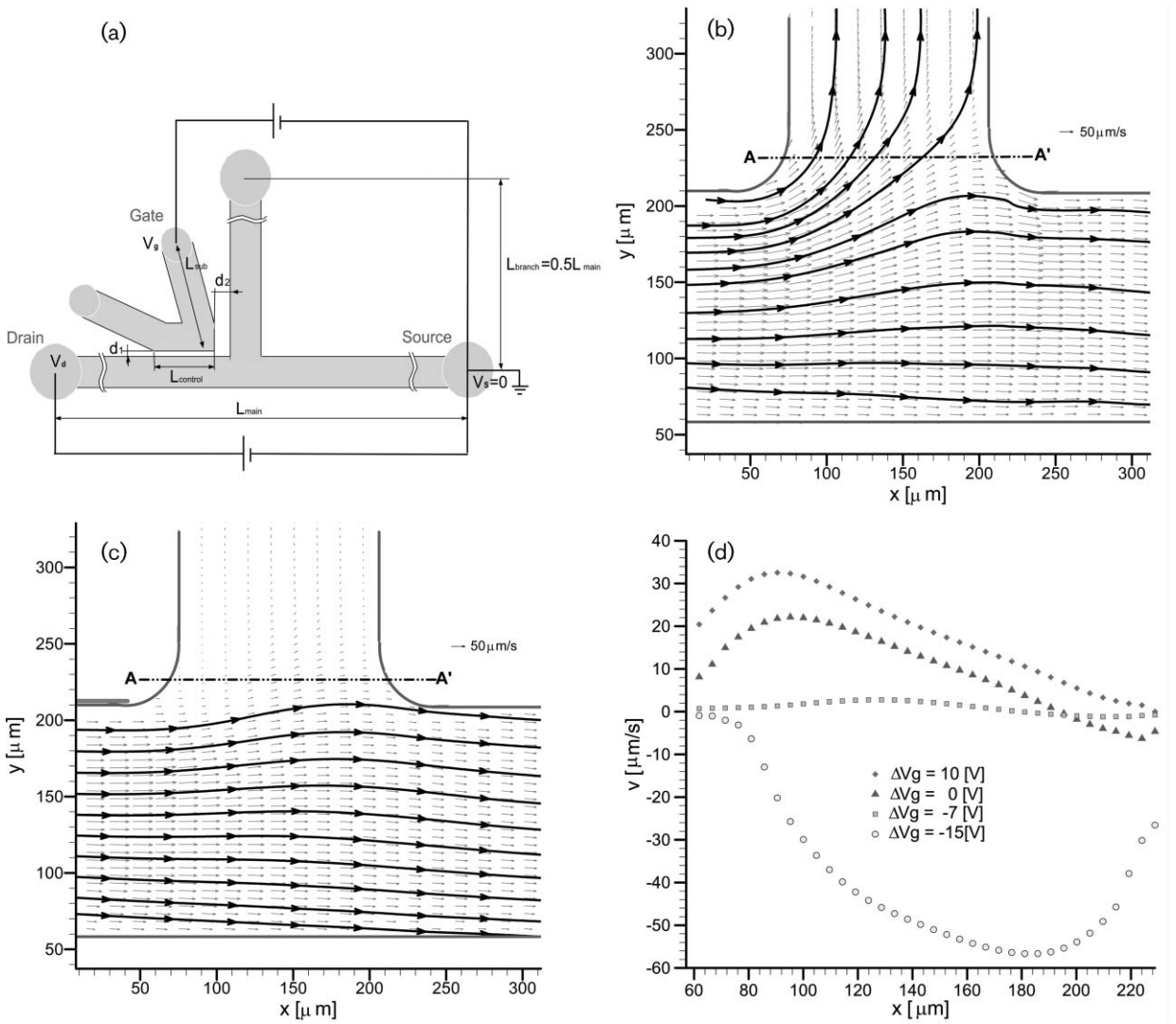

Fig. 7 (a) Schematic view of experimental setup to control flow at T-channel junction. The length, width and height of the main channel are 2 cm, 150 μm, and 10 μm, respectively. Vector plots of flow velocity in T-channel junction for (b) V_g = 25 V and (c) V_g = 18 V. (d) Cross-stream (v) velocity distribution at the entry of the branch channel (along A–A′ line) for different values of gate potential. Here the reference gate voltage (V_{g0}) is 18 V, d_1 = 50 μm, d_2 = 125 μm, L_{sub} = 3 mm, $L_{control}$ = 1 mm.

higher flow rate in the branch channel. On the other hand, for $\Delta V_g = -15$ V (in Fig. 7(d)), fluid is coming out from the branch channel to the main channel due to over control. In this case, the controlled leakage-current from the gate voltage is more than geometric racetrack-effect near the first corner of the branch channel. Hence, this field-effect transistor can control the flow locally in a T-channel junction. This technology could be used to alter the flow in other microgeometries such as cross-channel junction and dog-leg channels by introducing multiple individually addressable transistors along the microchip. We plan to address those in future publications.

Conclusions

EOF controls are demonstrated in microgeometries using field-effect transistor. The microchannel structures and the field-effect transistors are formed on PDMS, while a glass slide is used to cover the channels. Flow controls in straight channel and T-channel junctions are obtained both qualitatively and quantitatively using an in-house micro scale particle image velocimetry technique. Experiments show that there is current leakage from sub-channel to primary channel if a potential is applied in the gate reservoir. Although the resistivity of PDMS and glass are very high, a small amount of current leakage (up to 20 nA) took place most likely through the interface between PDMS and glass surfaces due to their finite roughness or improper bonding. To explain the flow control at low gate voltage, a leakage capacitance model is proposed in this study.

In our PDMS-glass microchip, it is possible to control the flow locally with low gate voltage (less than 50 V) without having any fluid leakage. In a straight microchannel, secondary EOF in lateral direction was observed due to asymmetric zeta potential distribution. The flow velocities obtained from control experiments are in agreement with those calculated based on leakage capacitance model. Although this electrokinetic flow control mechanism could be used in a

number of microgeometries, we have particularly demonstrated the field-effect control in a T-channel junction. In this case, the amount of flow coming from or going into the branch can be controlled by simply adjusting the gate voltage which is located at the upstream of the branch channel. For an optimum gate voltage ($\Delta V_{gs} = -7$ V for our case), the net flow in the branch channel reaches zero.

The field-effect transistor presented in this study offers a number of important advantages over other exiting flow control transistors. First, it can control the flow locally at very low gate voltage even for a micron sized gap between main and sub-channel. Second, it offers very simple design, and it could be used to control flow in complex microgeometries. Third, this field-effect transistor formed on PDMS can be combined with other substrates such as glass, silicon wafer or quartz, as long as the substrate processes good electroosmotic characteristics.

Acknowledgements

The authors thank Professor Cornelius F. Ivory for sharing his knowledge of the capacitance model. This investigation was supported in part by the Washington State University Office of Research and in part by the National Science Foundation under Grant No. CTS0300802.

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